

FIG. 1

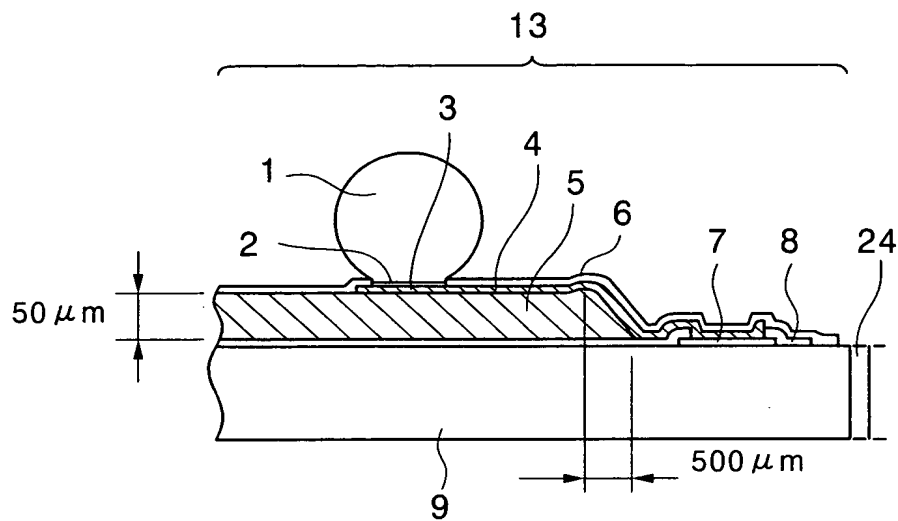


FIG. 2

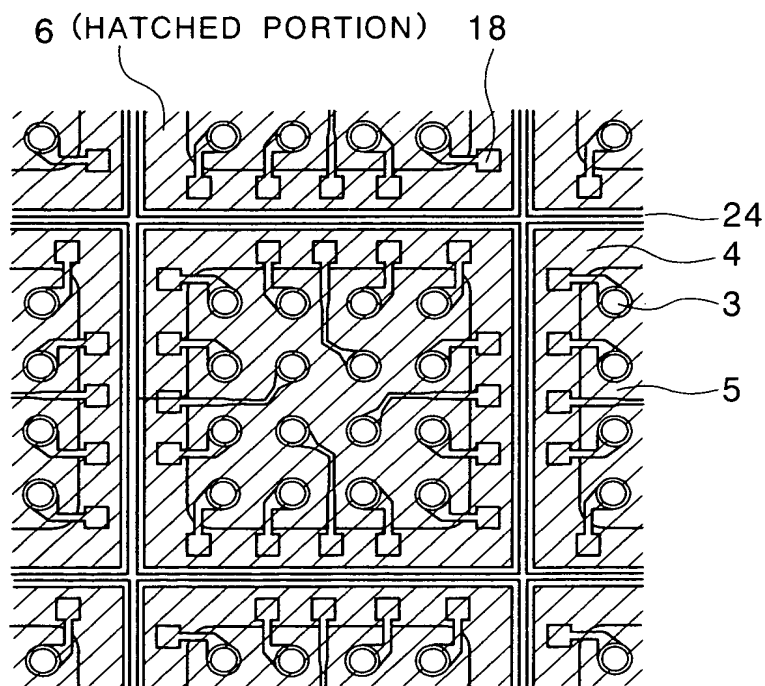


FIG. 3

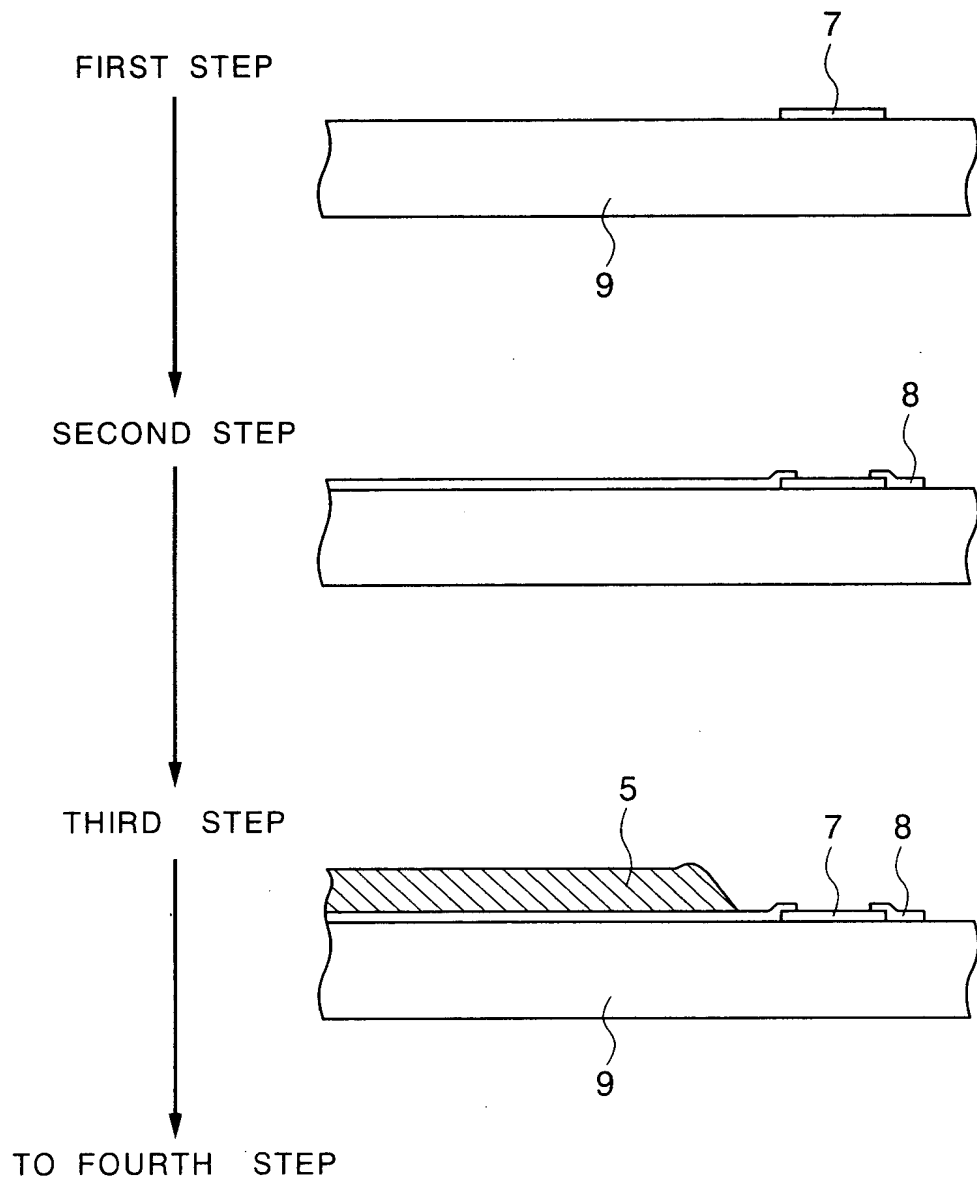


FIG. 4

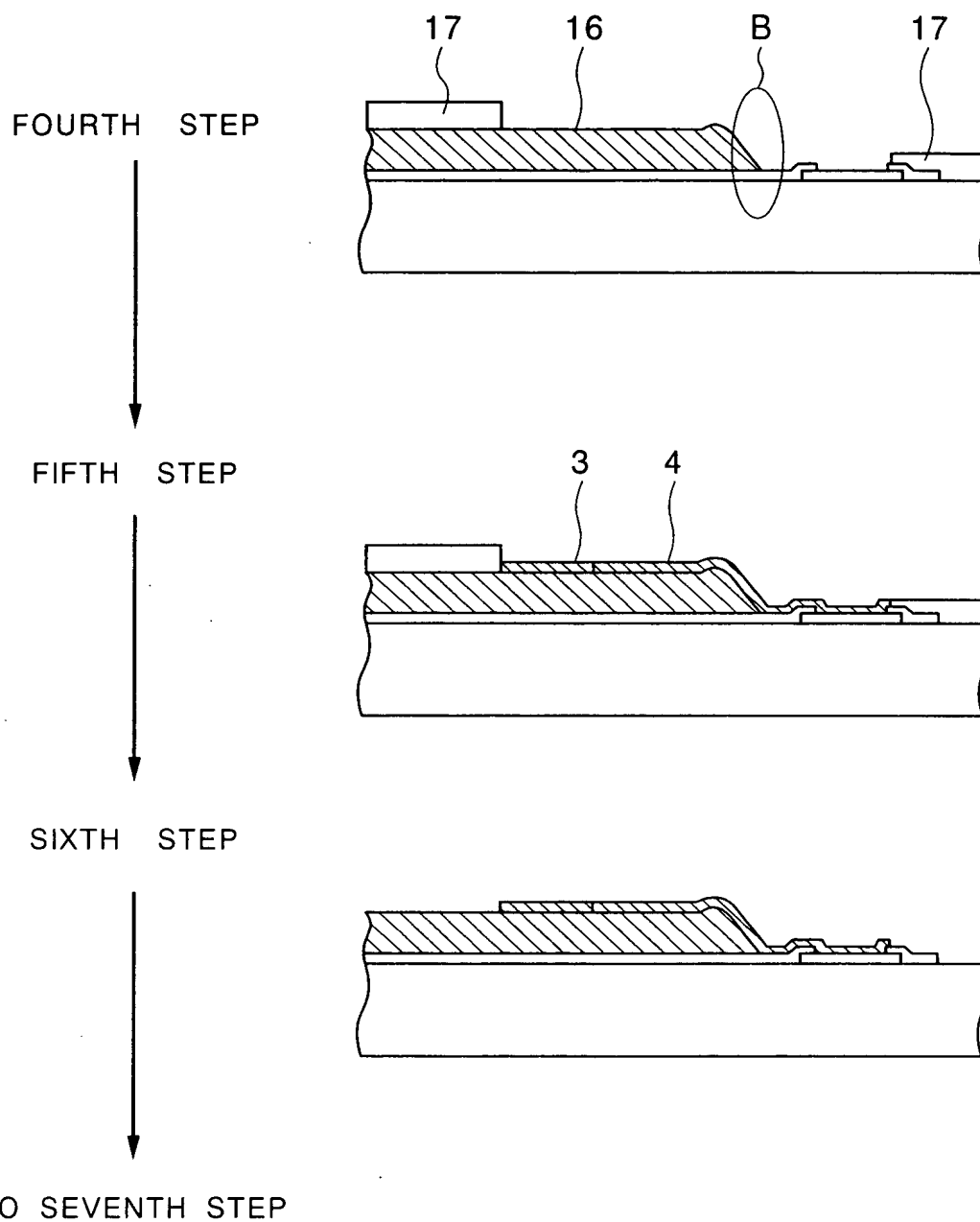
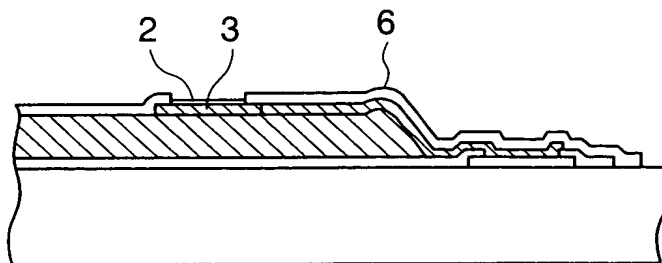
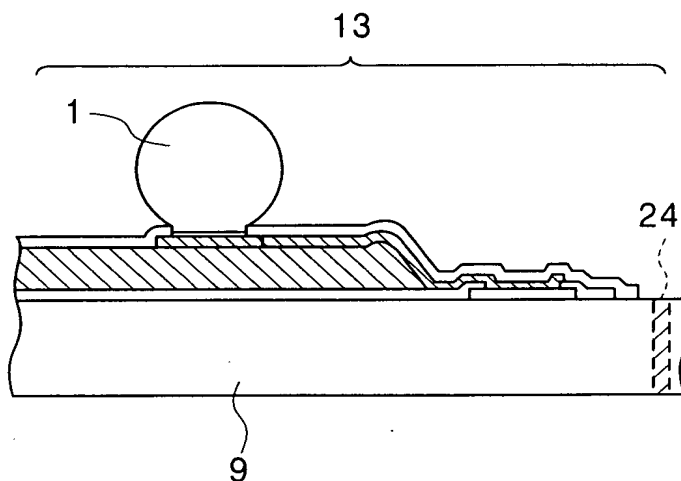


FIG. 5

SEVENTH STEP



EIGHTH AND  
NINTH STEP



COMPLETE



FIG. 9

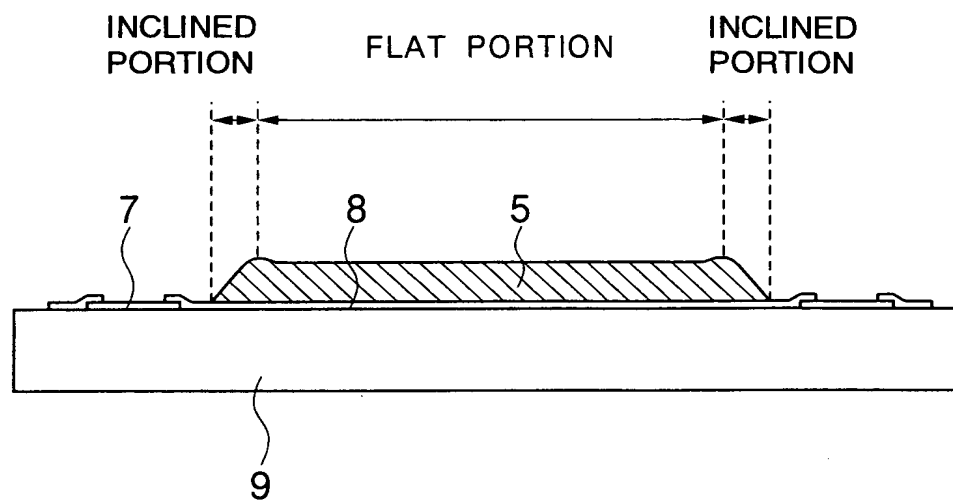


FIG. 10

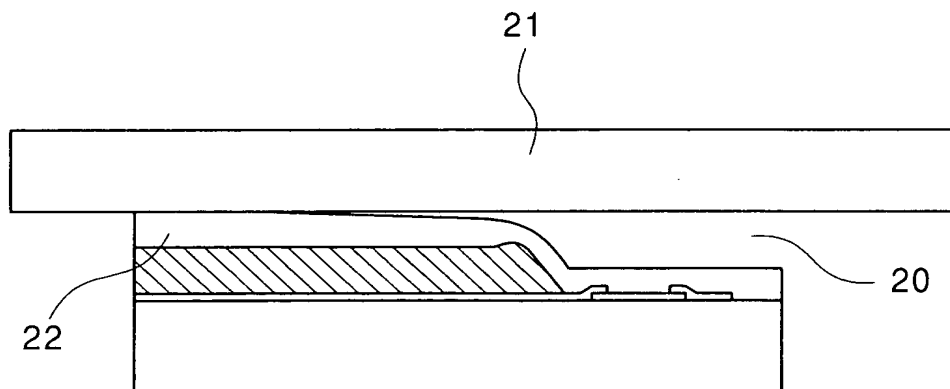


FIG. 11

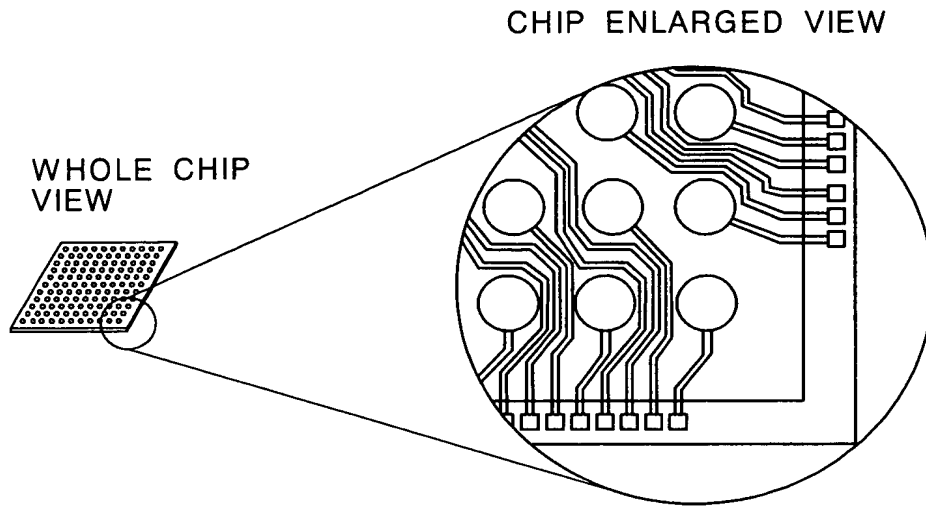


FIG. 12

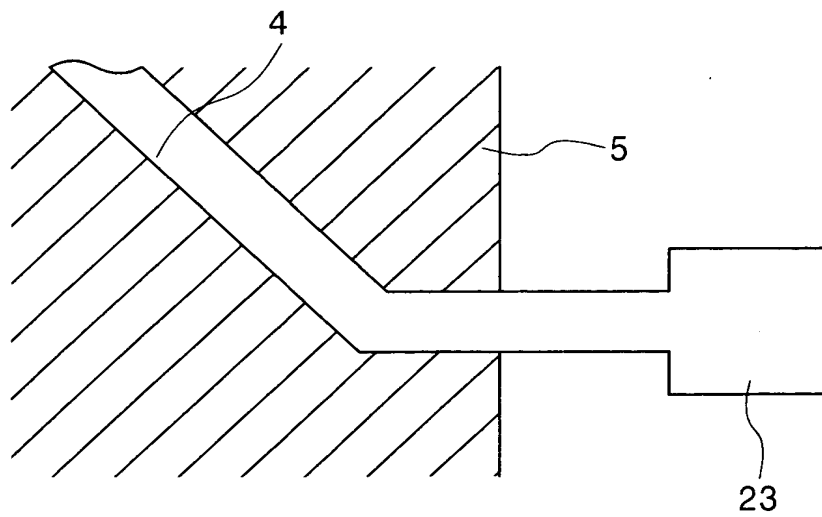


FIG. 13

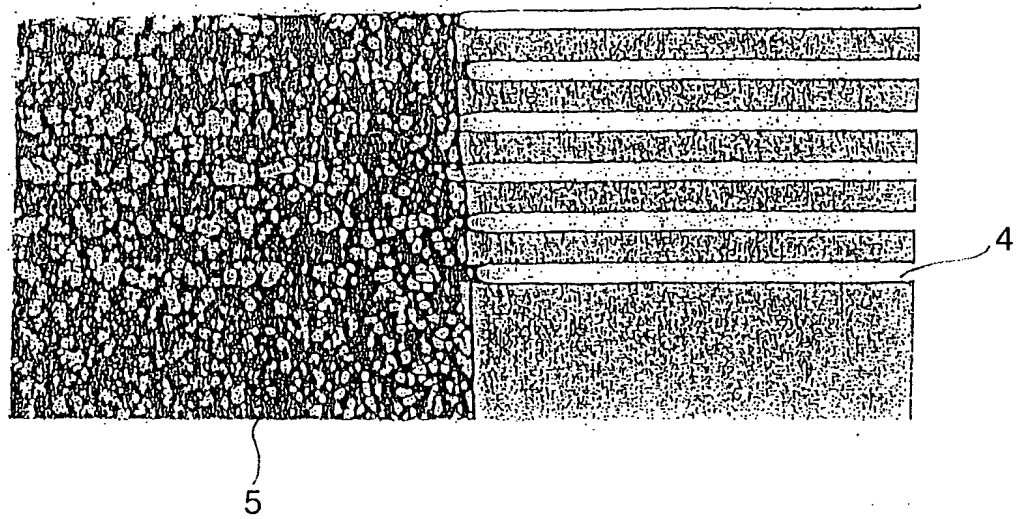


FIG. 14

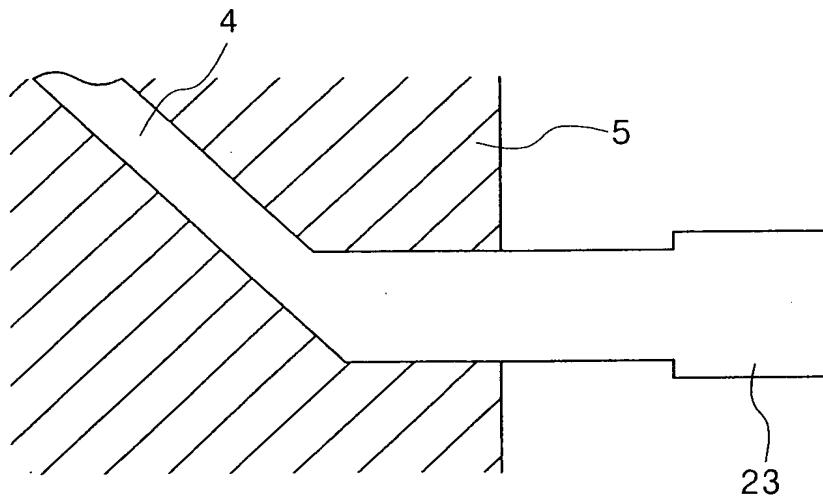




FIG. 15

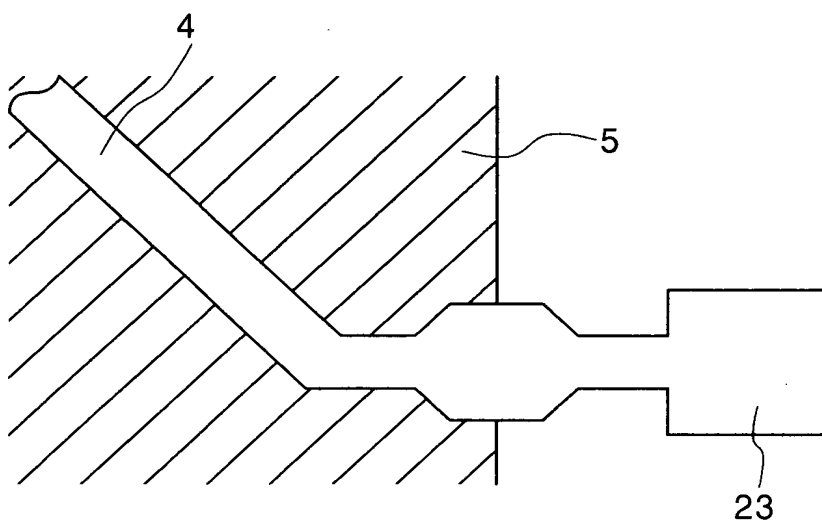
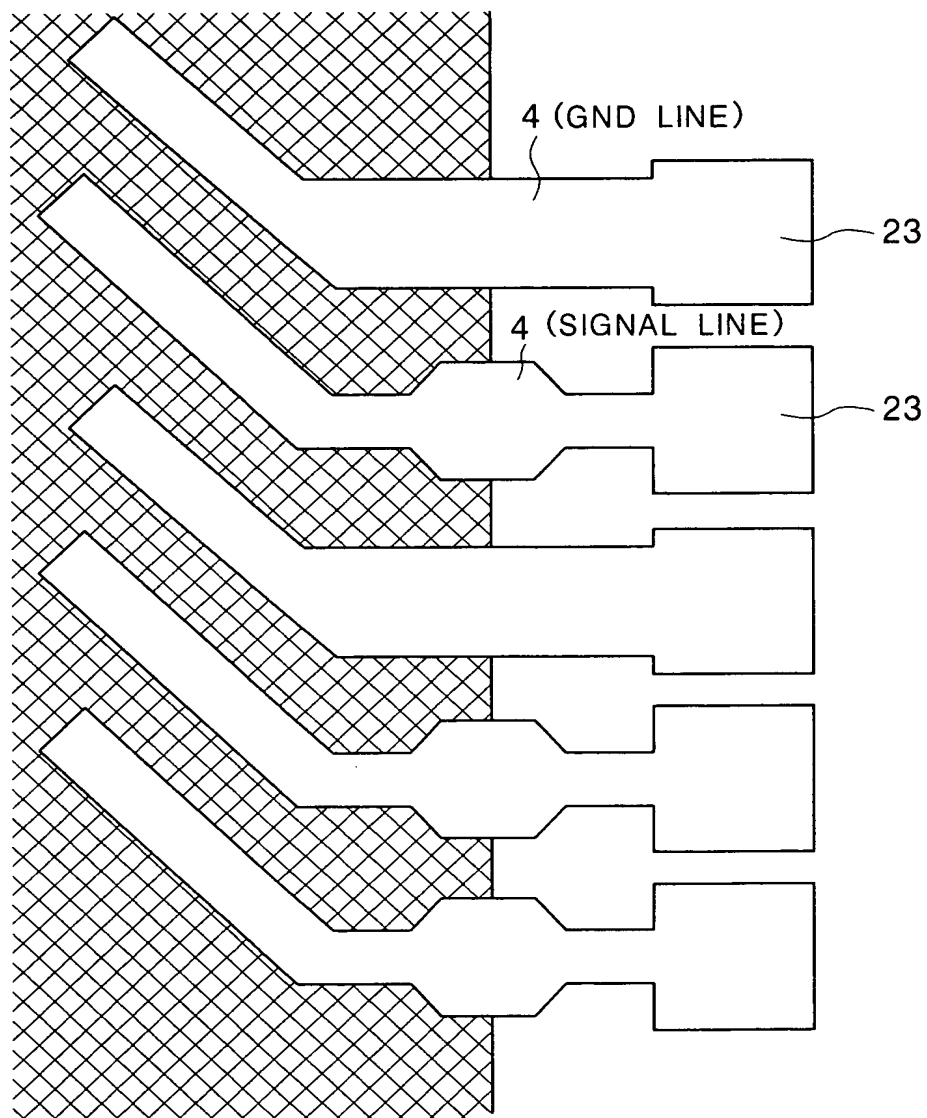


FIG. 16



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FIG. 17

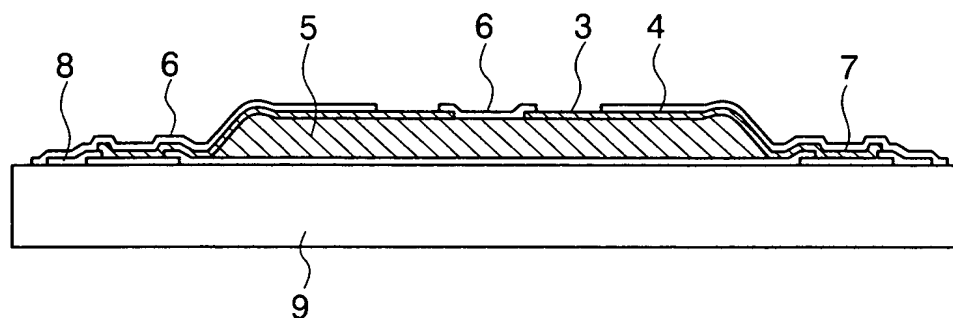
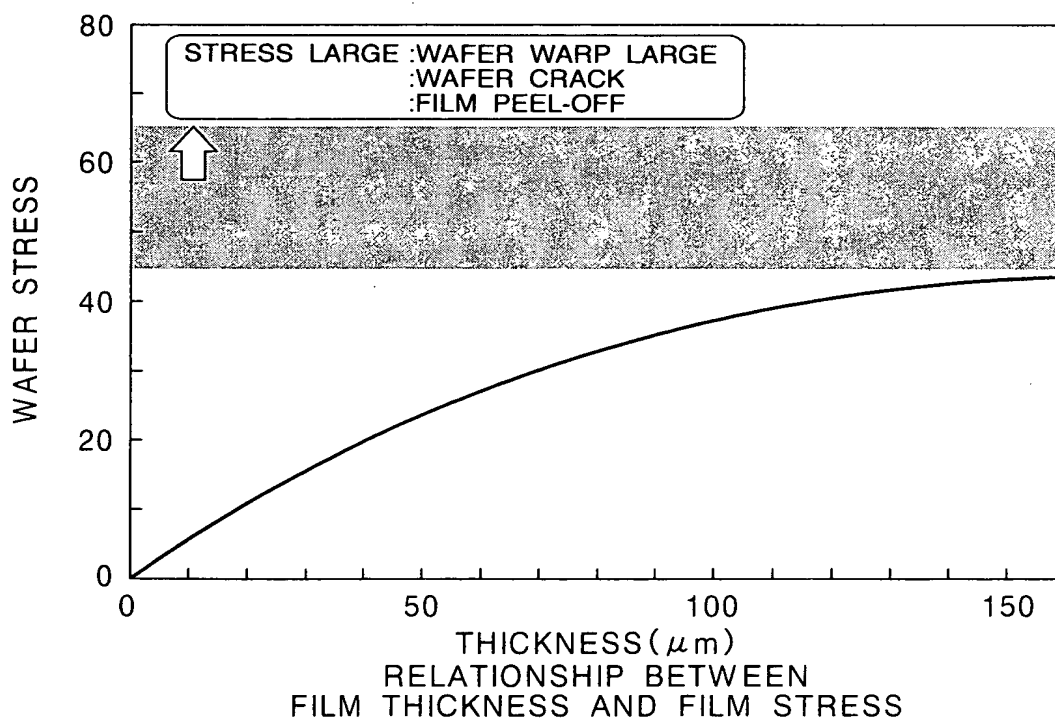


FIG. 18



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FIG. 19

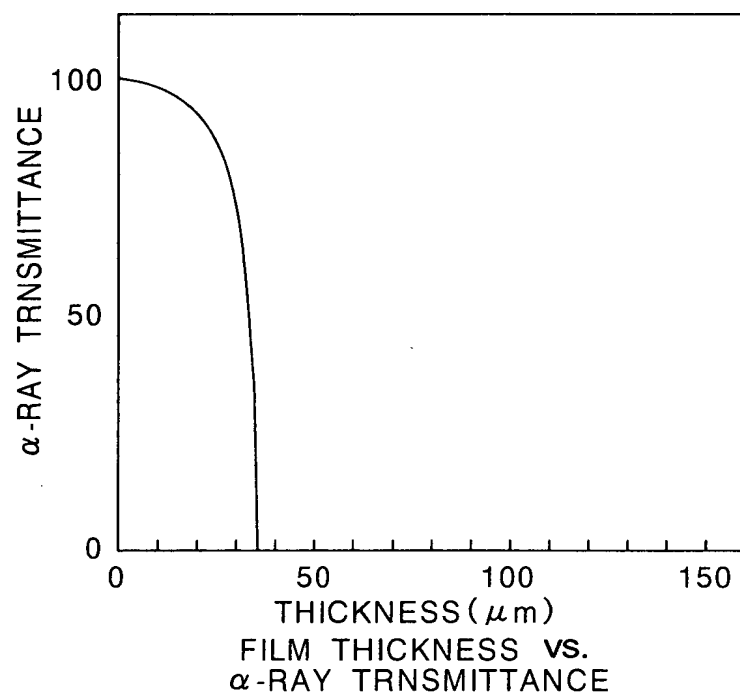
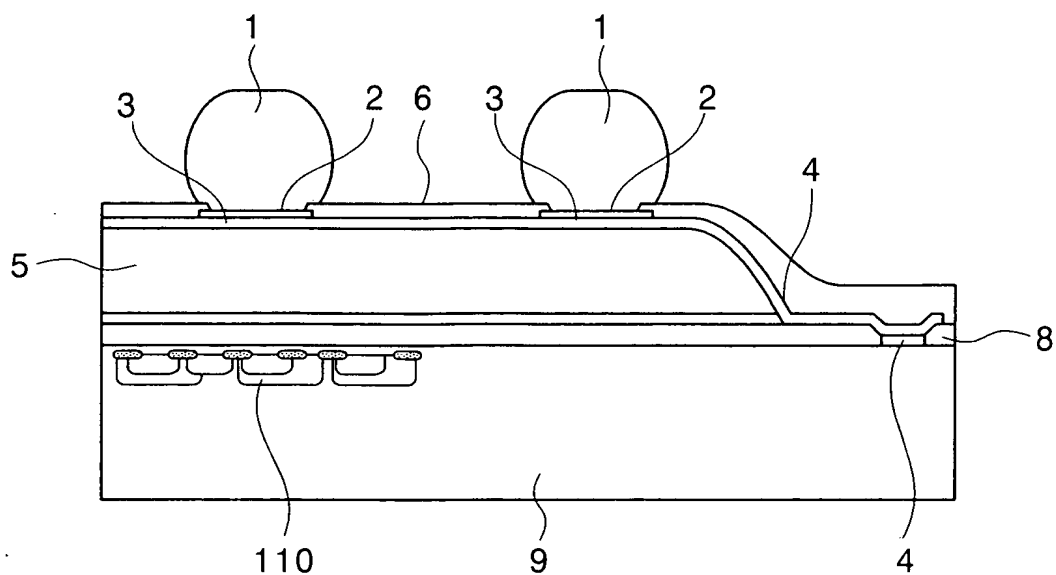


FIG. 20



This diagram shows a cross-sectional view of a semiconductor device. Two semiconductor elements, labeled 1, are mounted on a substrate 9. Each element 1 is connected to a pad 2, which is in turn connected to a conductive layer 3. The conductive layer 3 is part of a larger structure 4 that extends across the device. A layer 5 is located beneath the conductive layer 3. A layer 6 is located beneath the conductive layer 4. A layer 7 is located beneath the layer 6. A layer 8 is located beneath the layer 7. The substrate 9 is the base of the device.

A cross-sectional view of a semiconductor device 100. The device includes a substrate 1, a gate stack 2, 3, a channel region 4, a source/drain region 5, and a contact 6. A dashed line 102 indicates a boundary or interface.

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FIG. 23

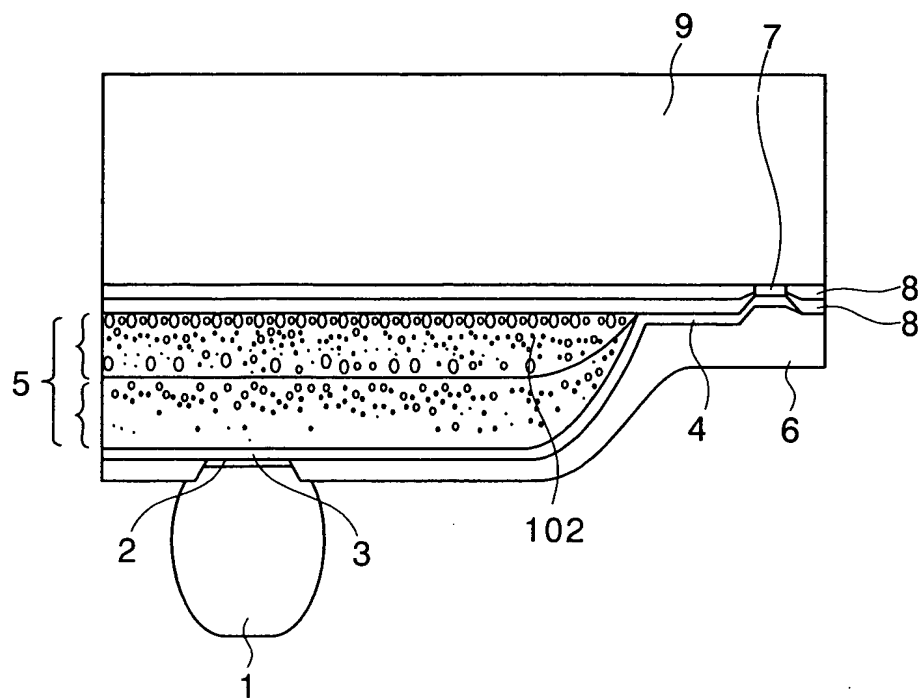


FIG. 24

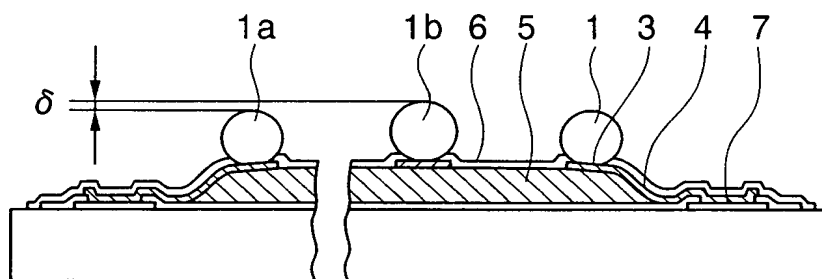


FIG. 25

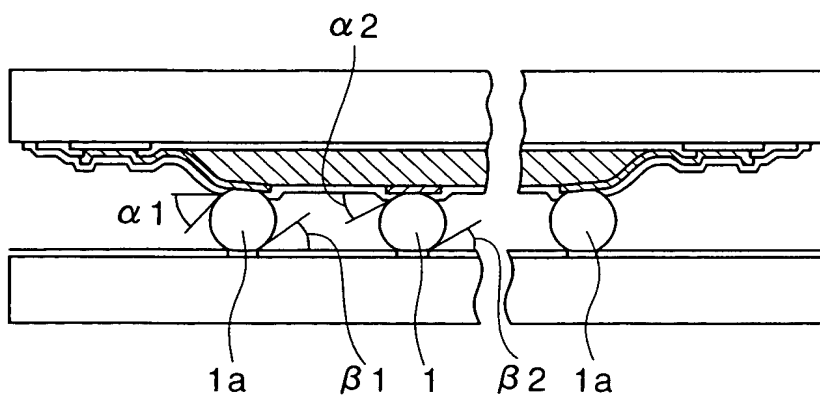


FIG. 26a

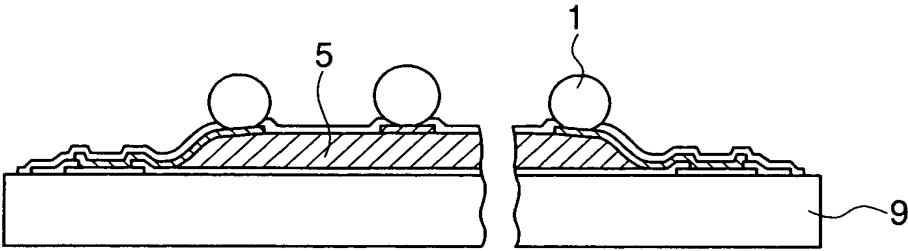


FIG. 26b

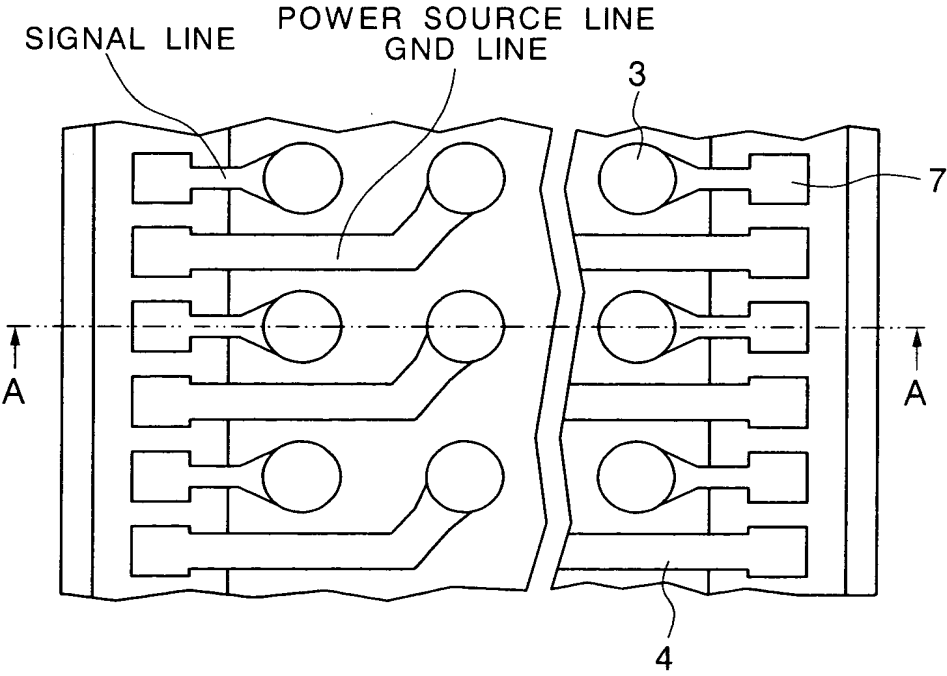


FIG. 27

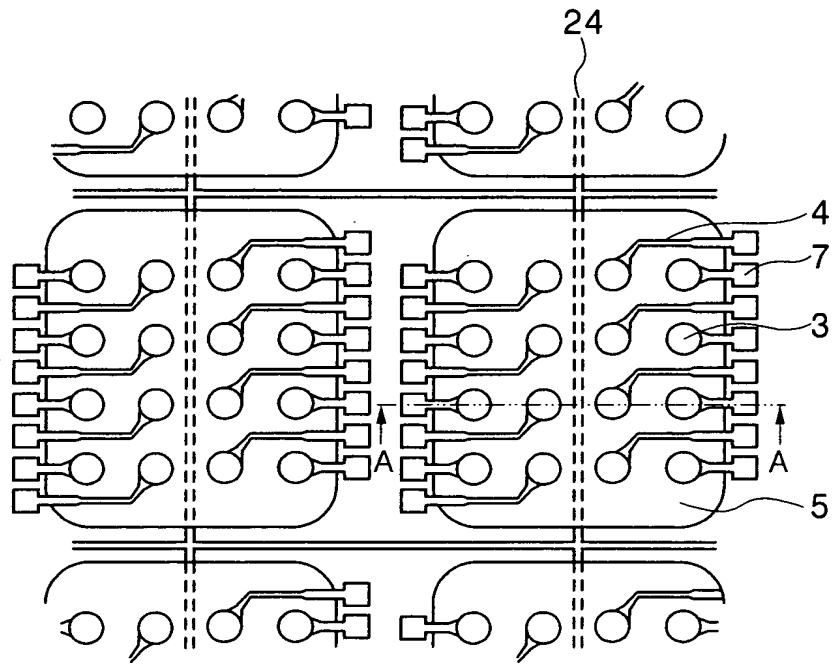




FIG. 28

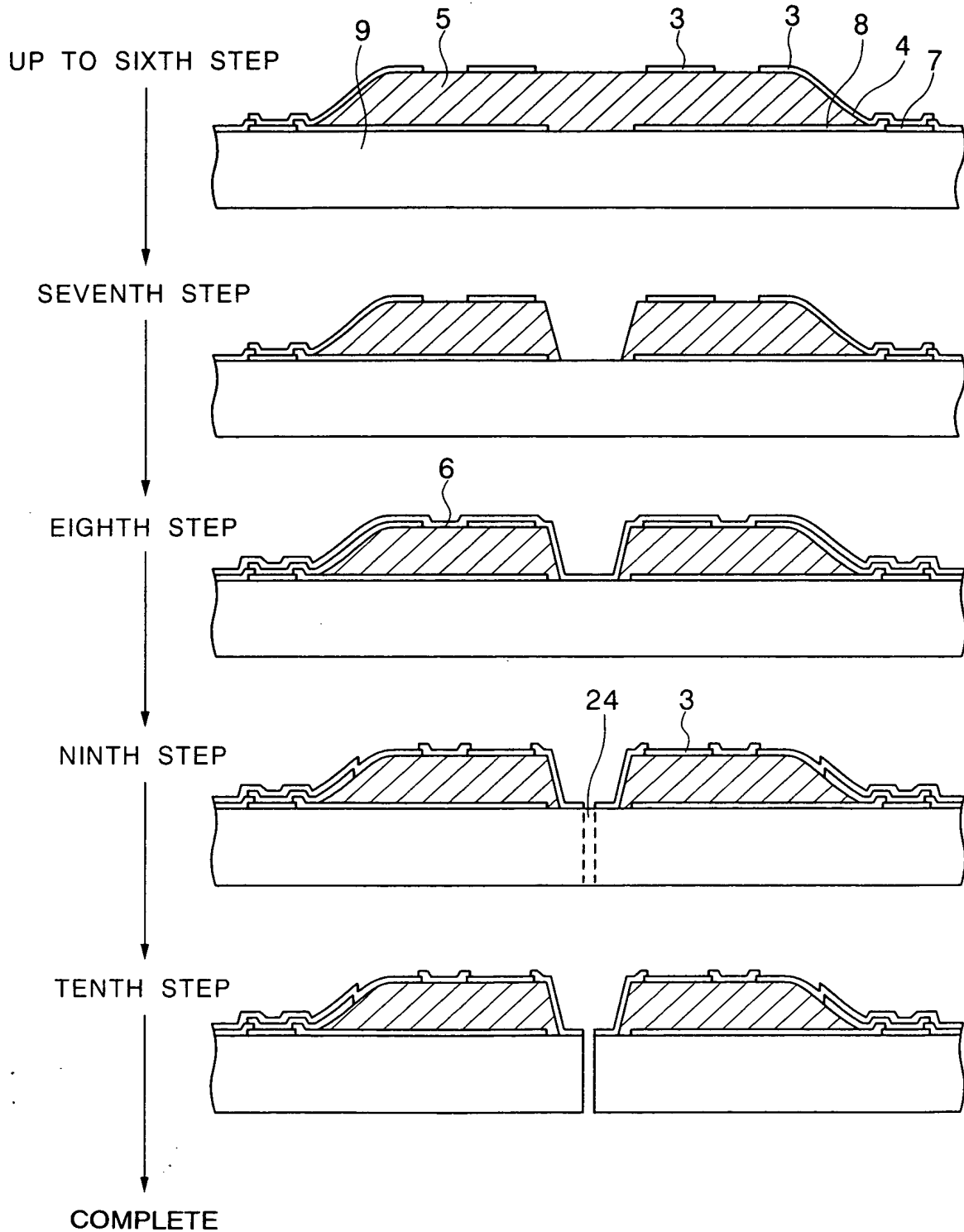


FIG. 29

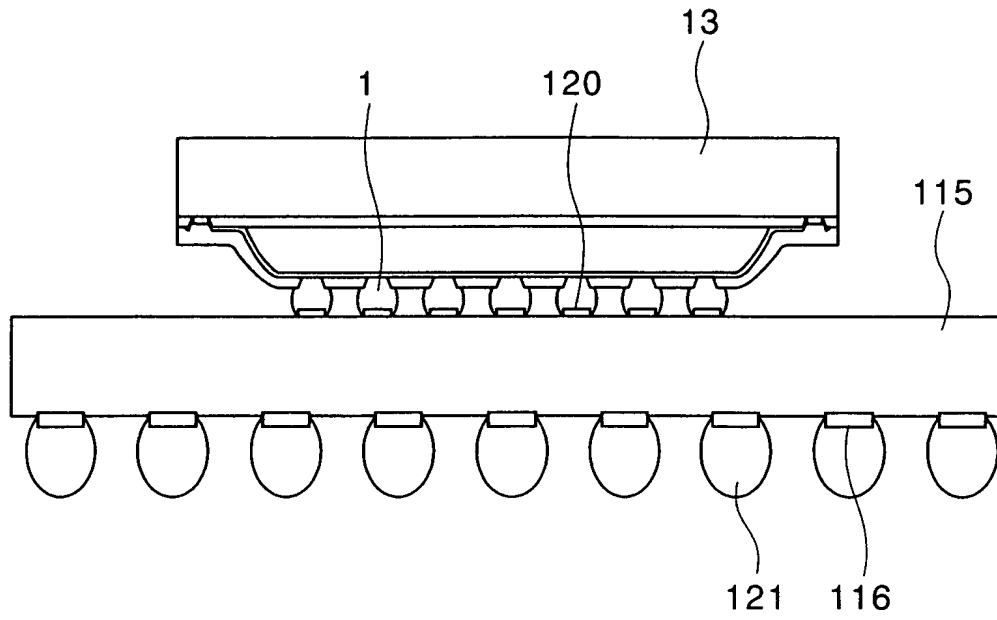


FIG. 30

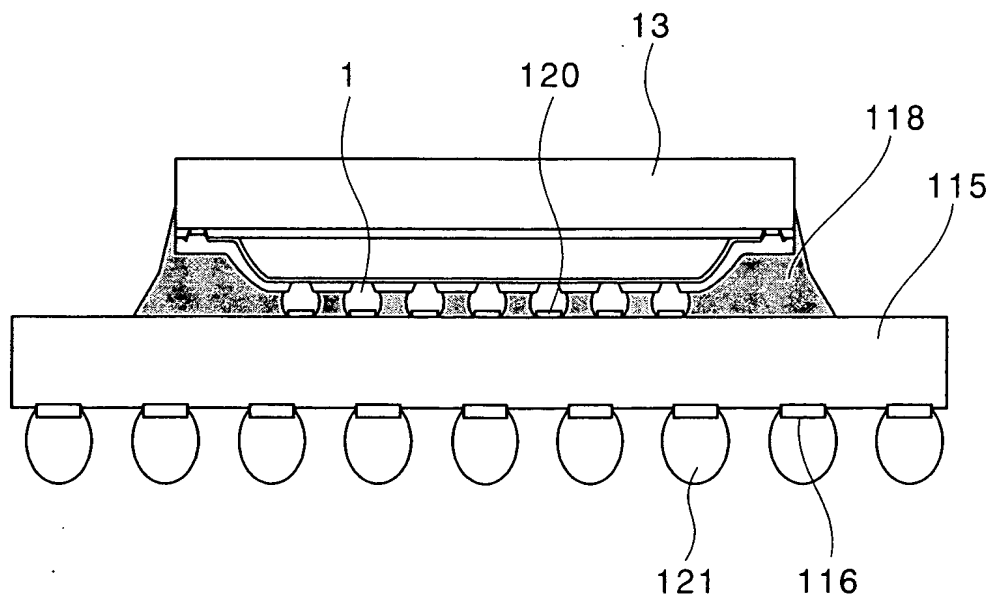


FIG. 31

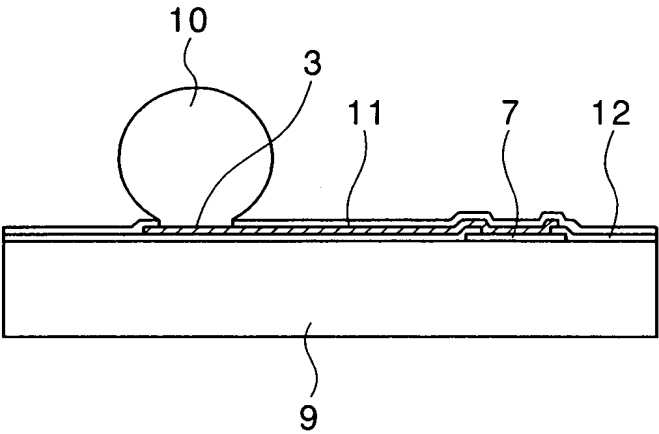


FIG. 32

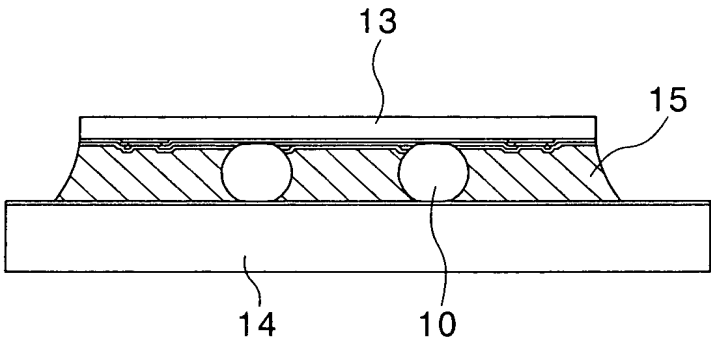


FIG. 33a

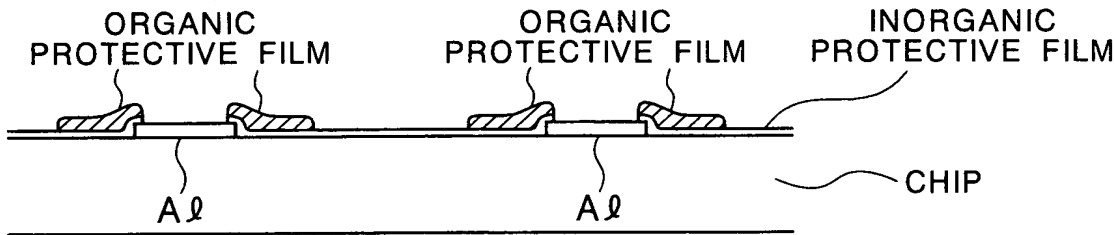


FIG. 33b

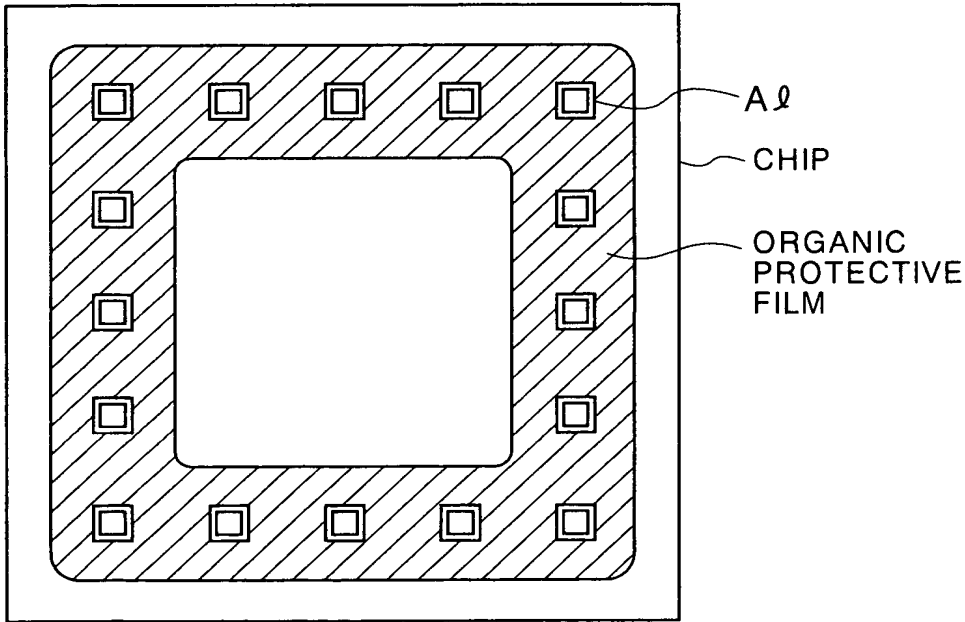


FIG. 34a

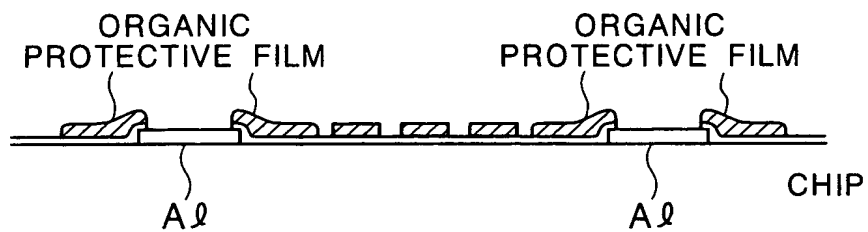


FIG. 34b

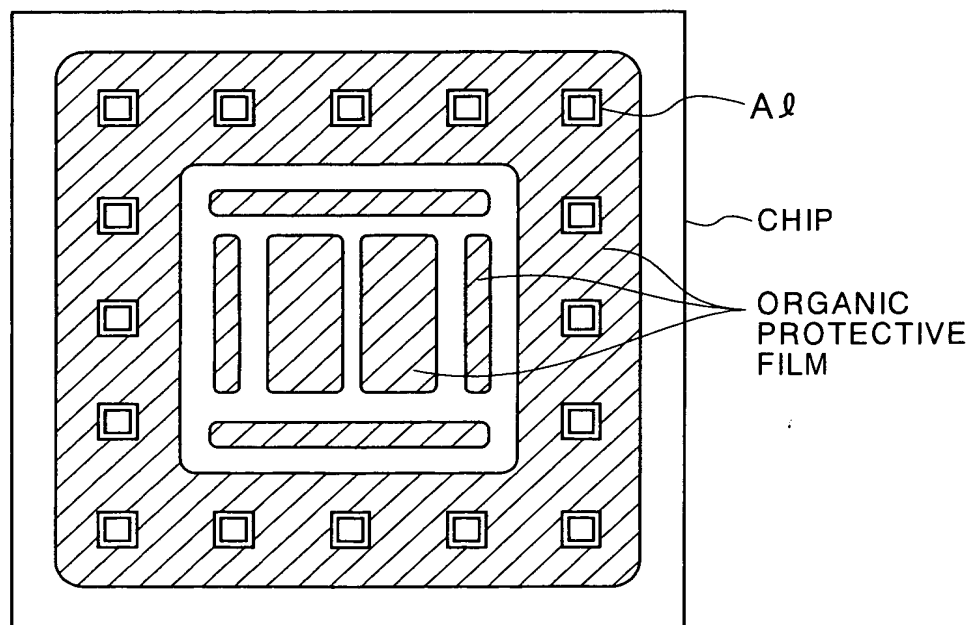
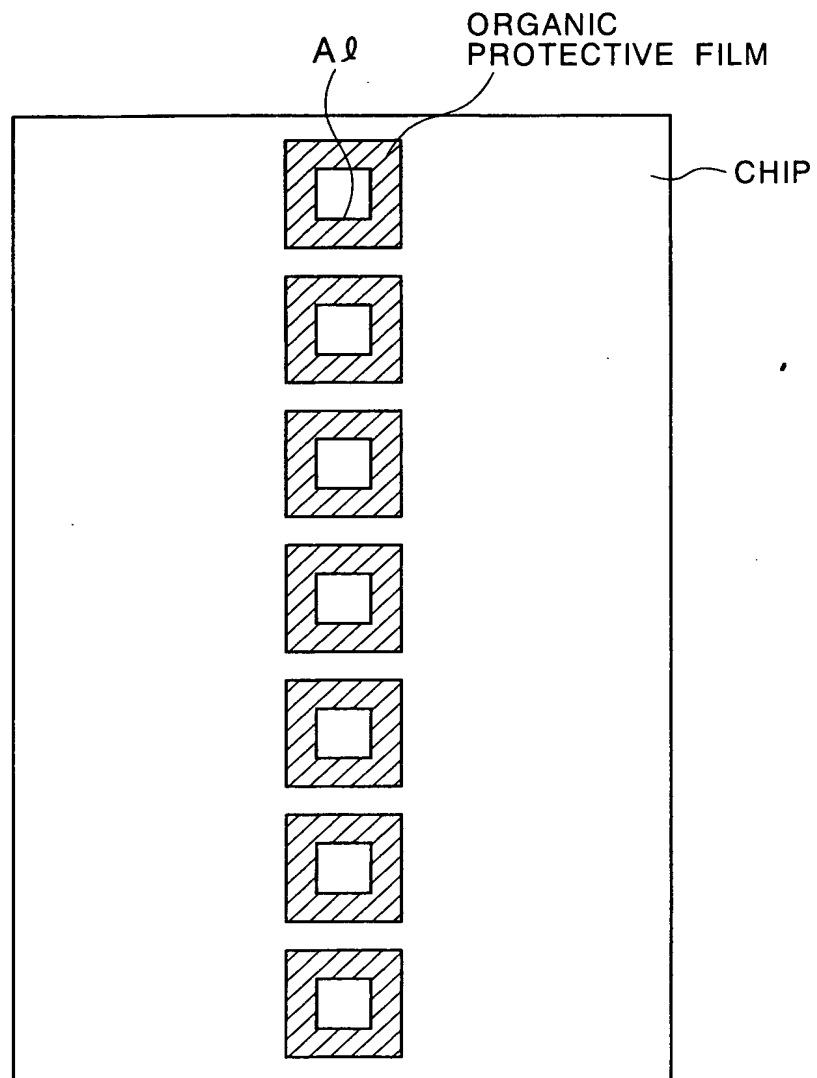


FIG. 35



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FIG. 36

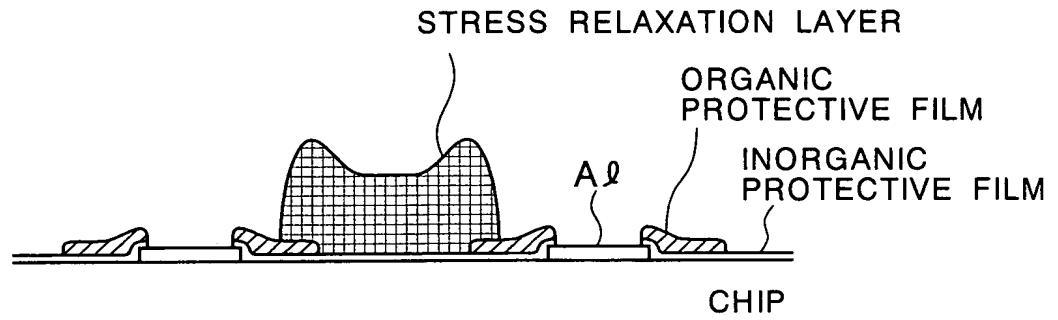


FIG. 37

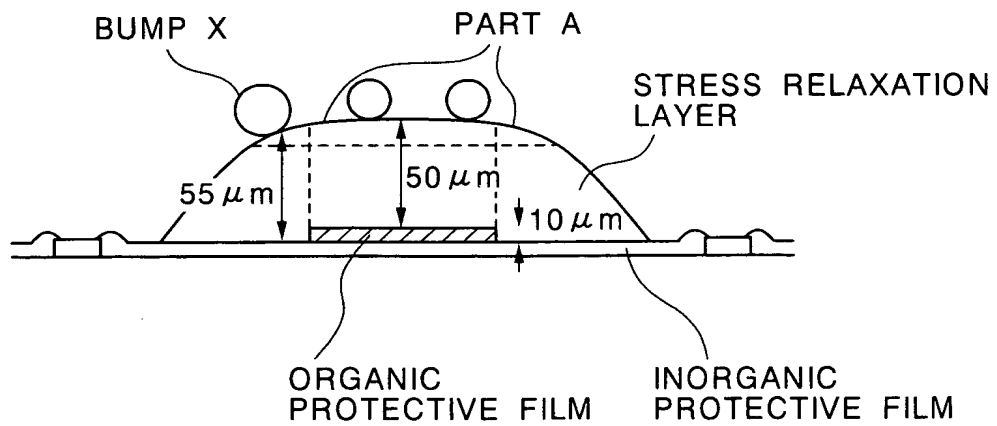


FIG. 38

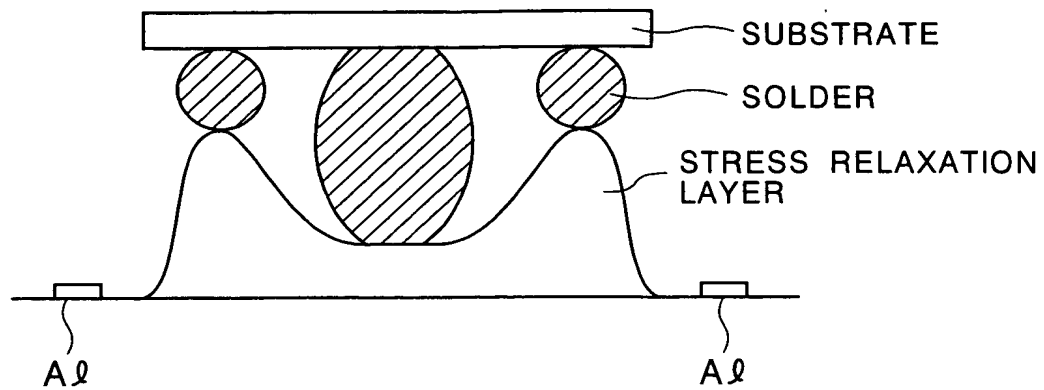


FIG. 39a

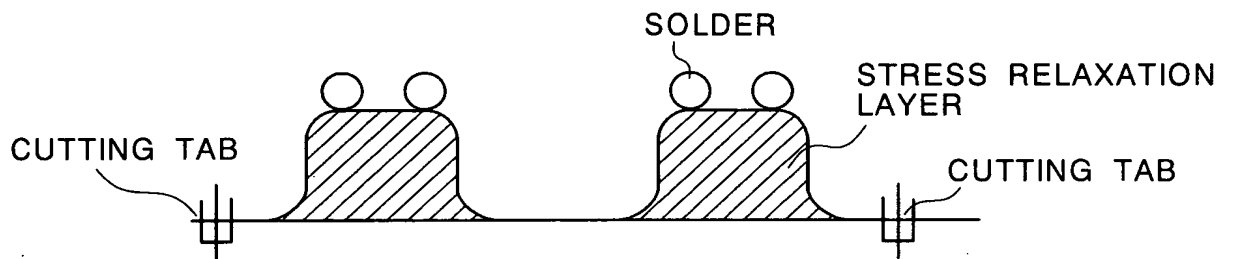


FIG. 39b

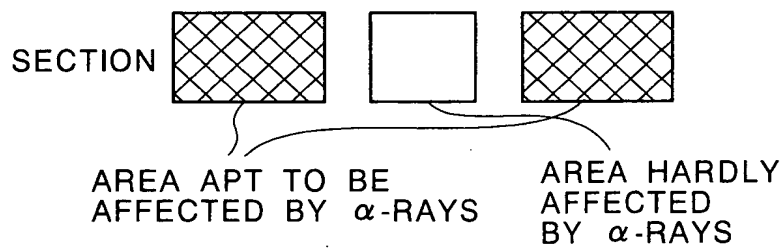


FIG. 39c

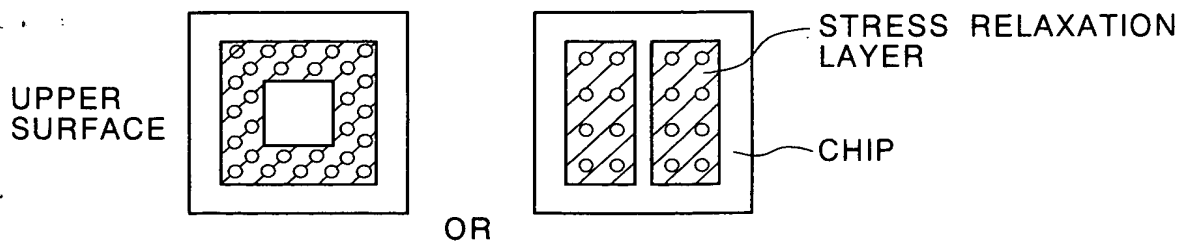




FIG. 40

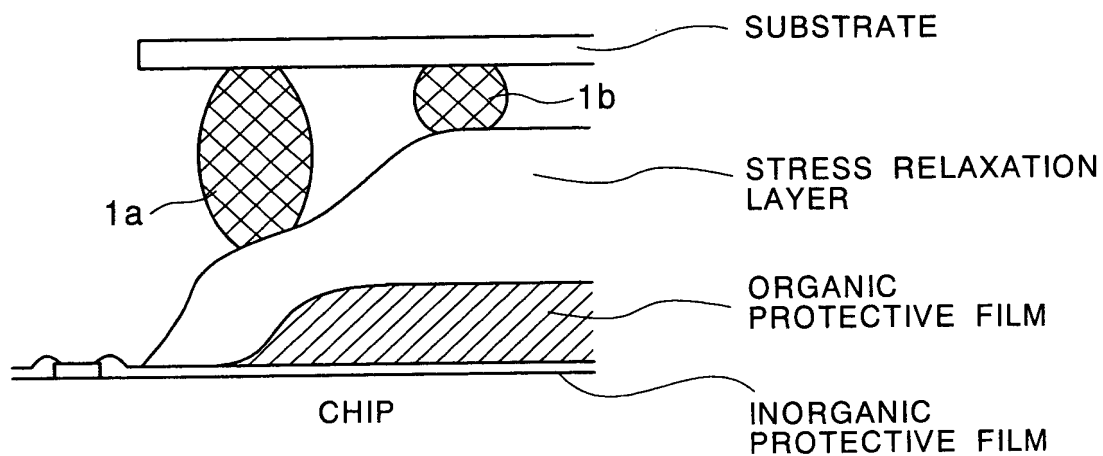


FIG. 41

